

A hand-drawn schematic diagram of a CMOS inverter cross-section. The diagram shows a rectangular substrate labeled '14' with an 'N-WELL' region. Inside the N-well, there are two p+ regions labeled '16' and '18', and one n+ region labeled '28'. A gate stack is shown on top of the p+ regions, with a gate layer labeled '20' and a gate oxide layer labeled '22'. The gate is connected to a terminal 'S' (source) and a terminal 'D' (drain). The drain is connected to a terminal 'Vcc' and a terminal 'SUB' (substrate) labeled '12'. A label '24' points to the p+ region under the gate. A label '26' points to the gate oxide layer. A label '10' points to the gate stack. A label '5' points to the source terminal. A label '6' points to the substrate. A label '7' points to the N-well. A label '8' points to the p+ region. A label '9' points to the n+ region.

TO LOWER VOLTAGES

FIG. 2

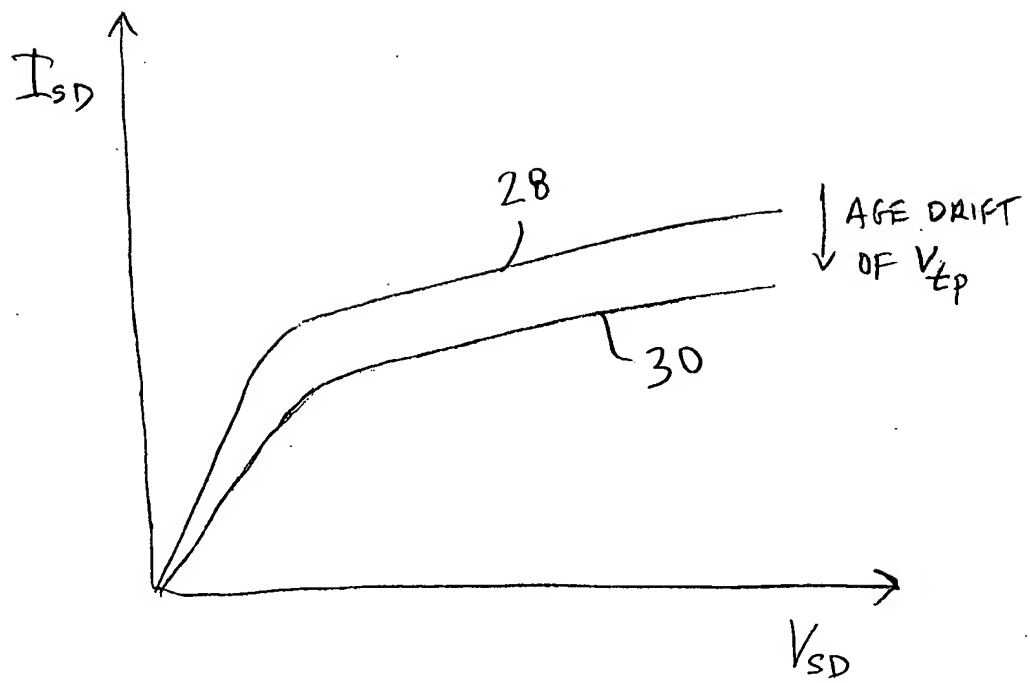


FIG. 3

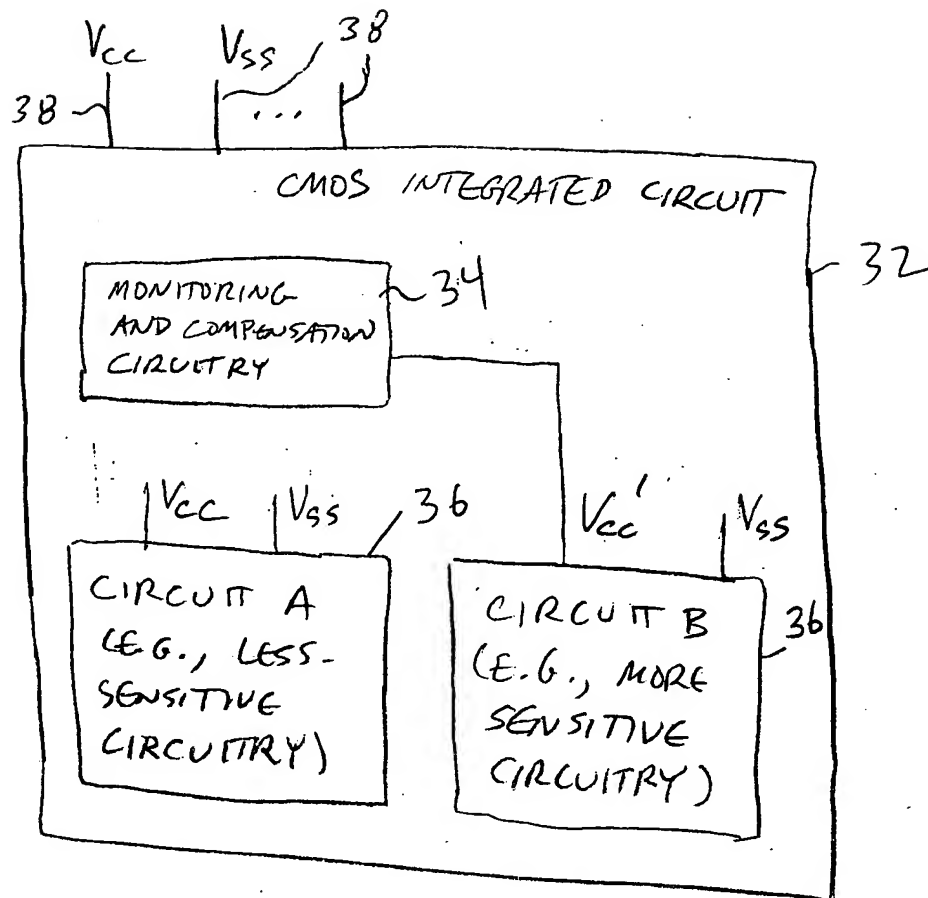


FIG. 4

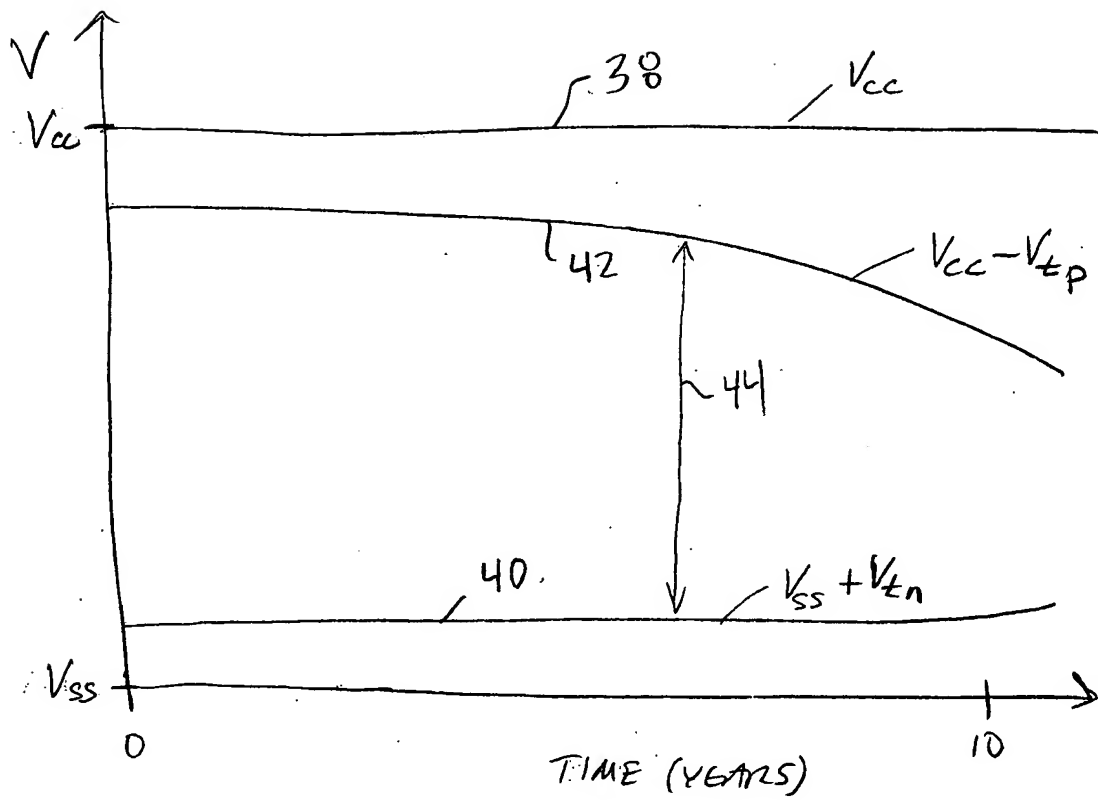


FIG. 5

— PRIOR ART —

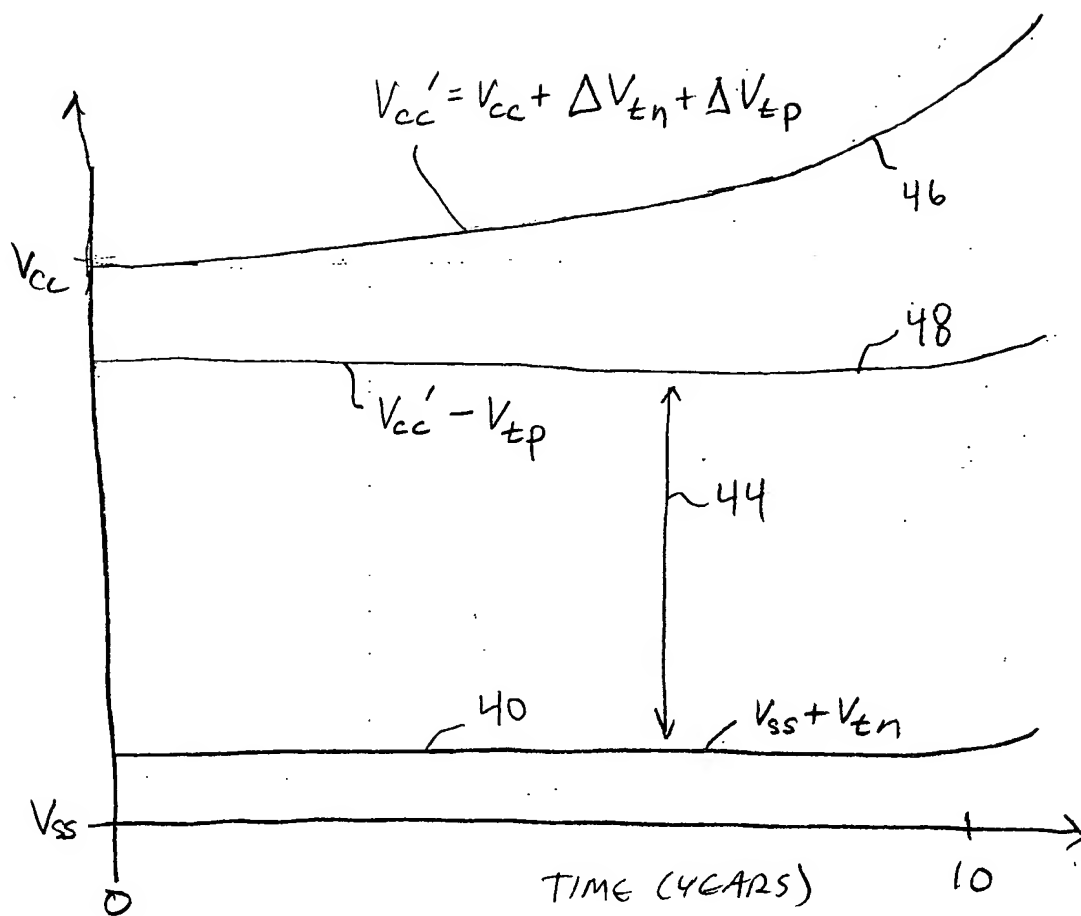


FIG. 6

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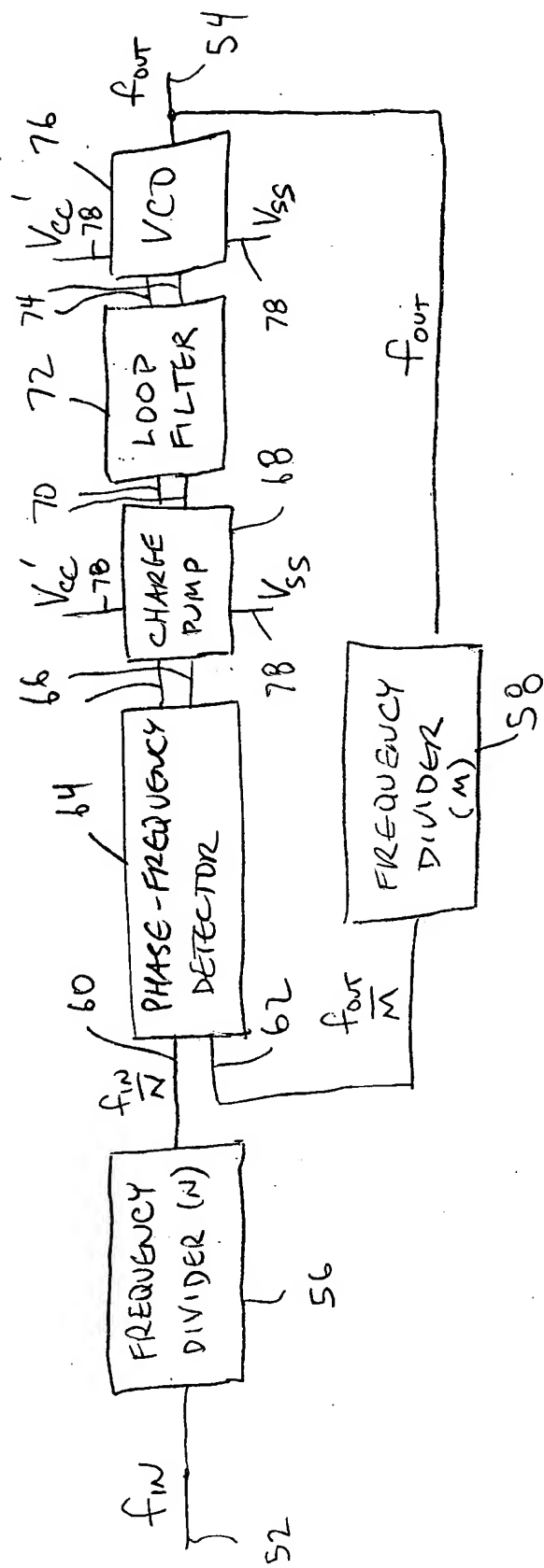


FIG. 7

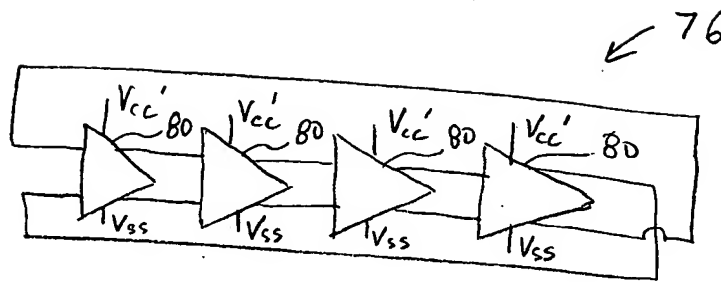


FIG. 8

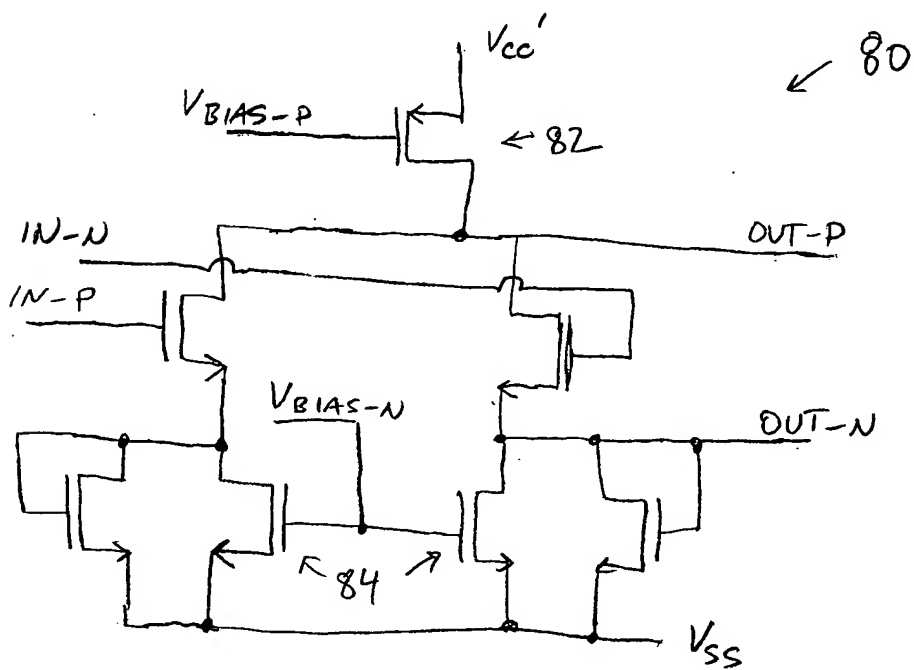


FIG. 9

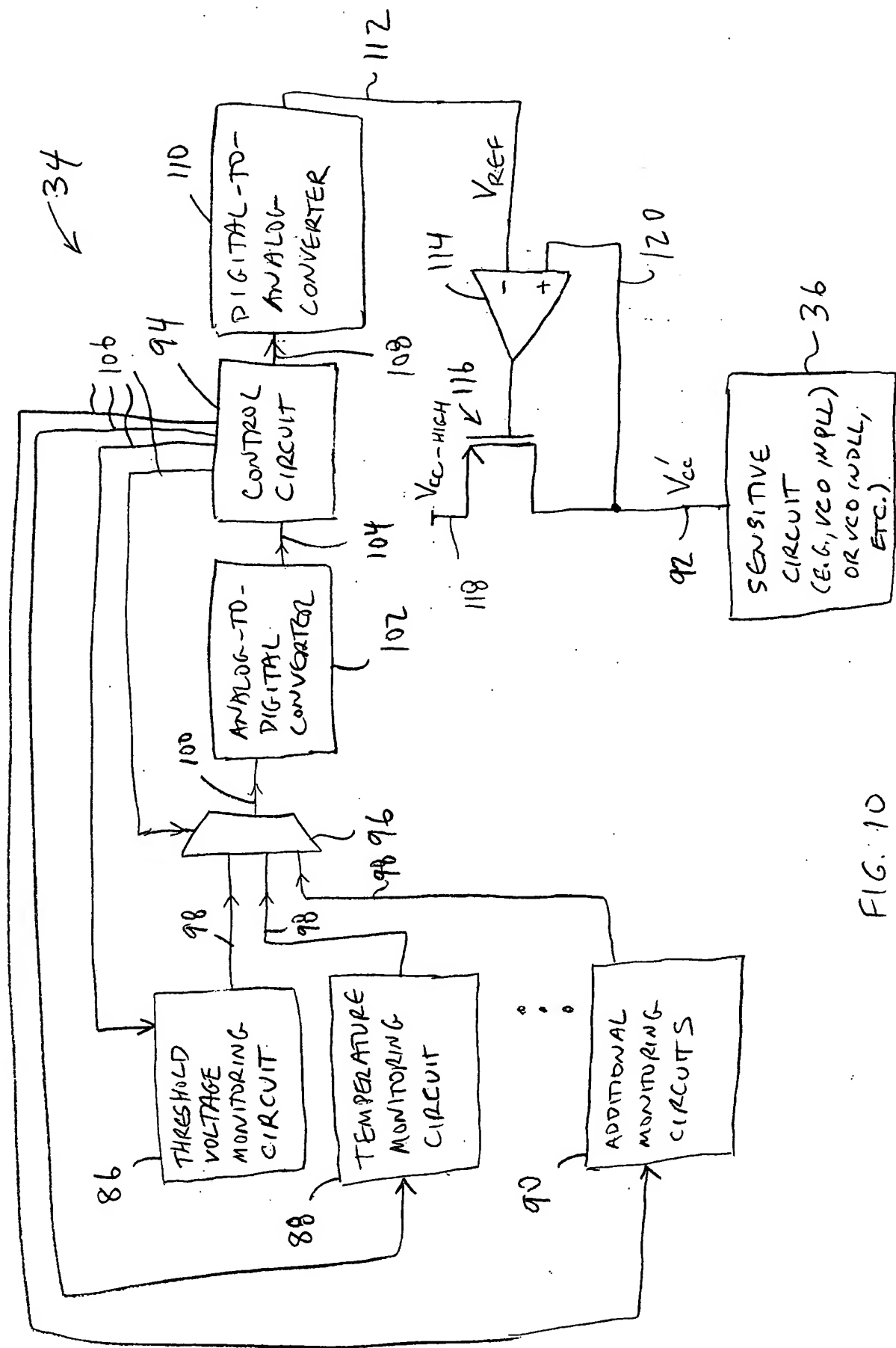


FIG. 10



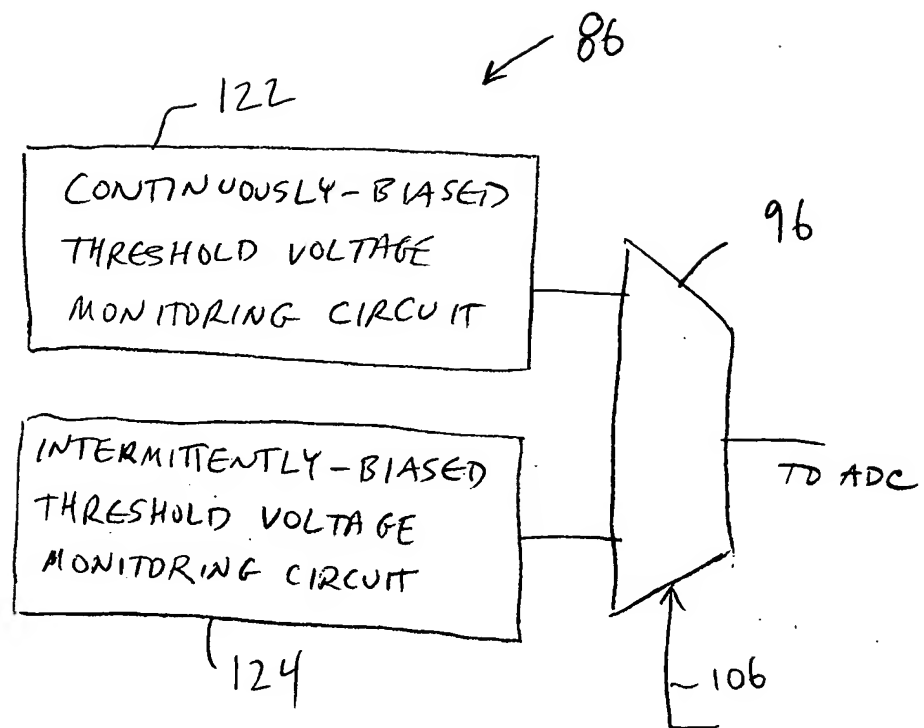


FIG. 11

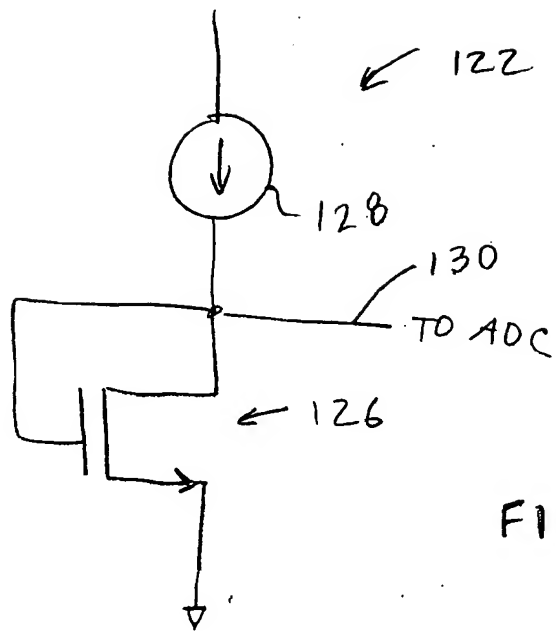


FIG. 12

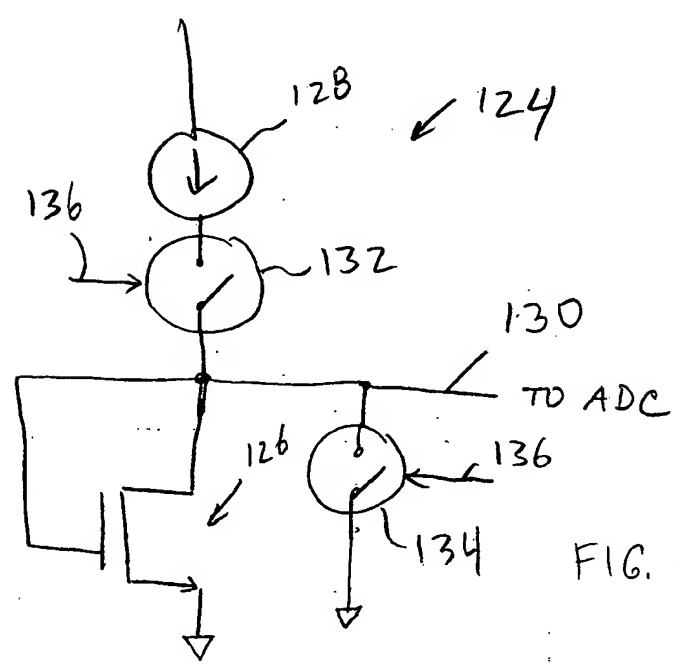
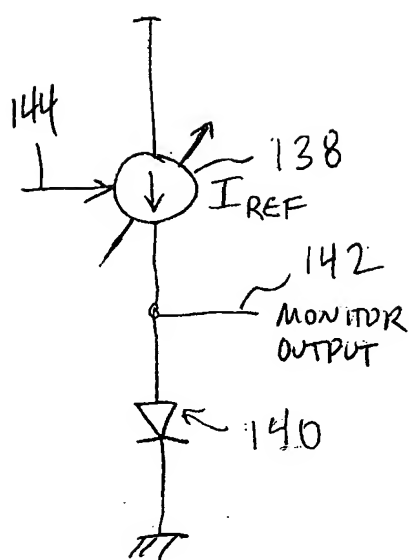


FIG. 13



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FIG. 14

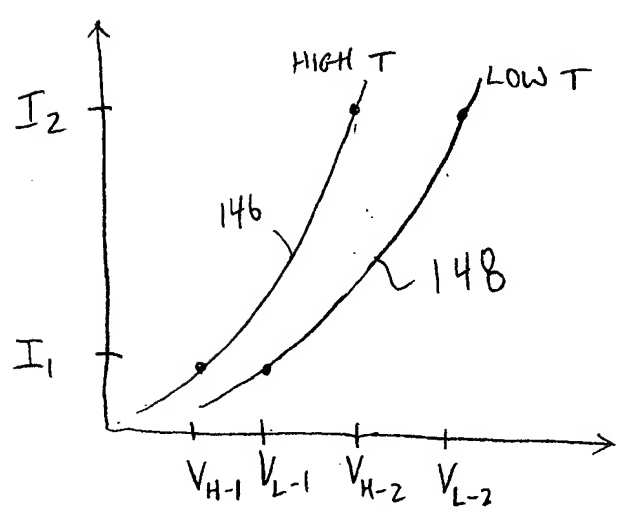


FIG. 15

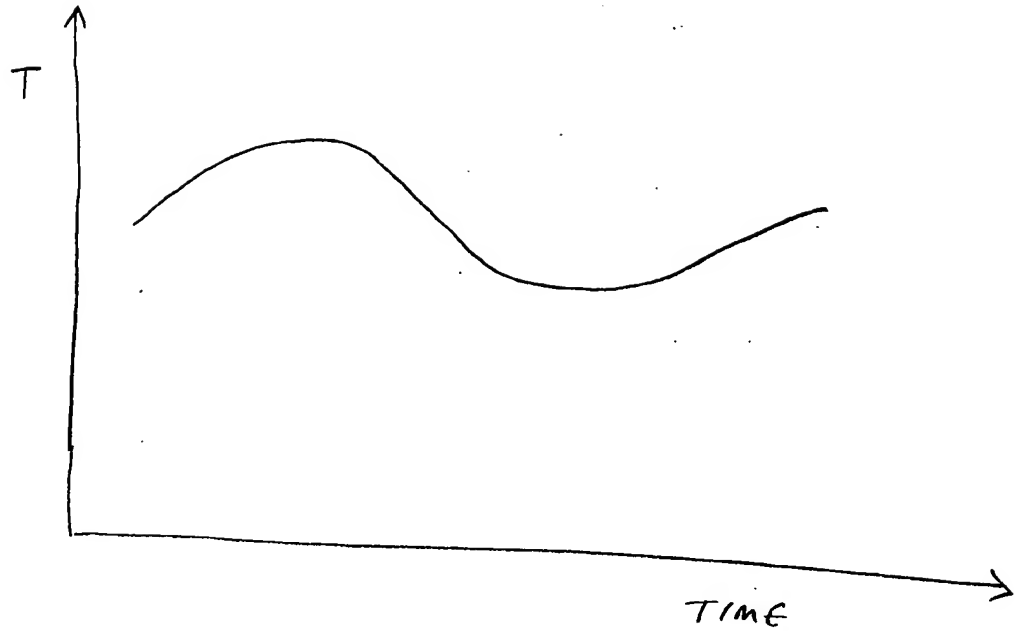


FIG. 16

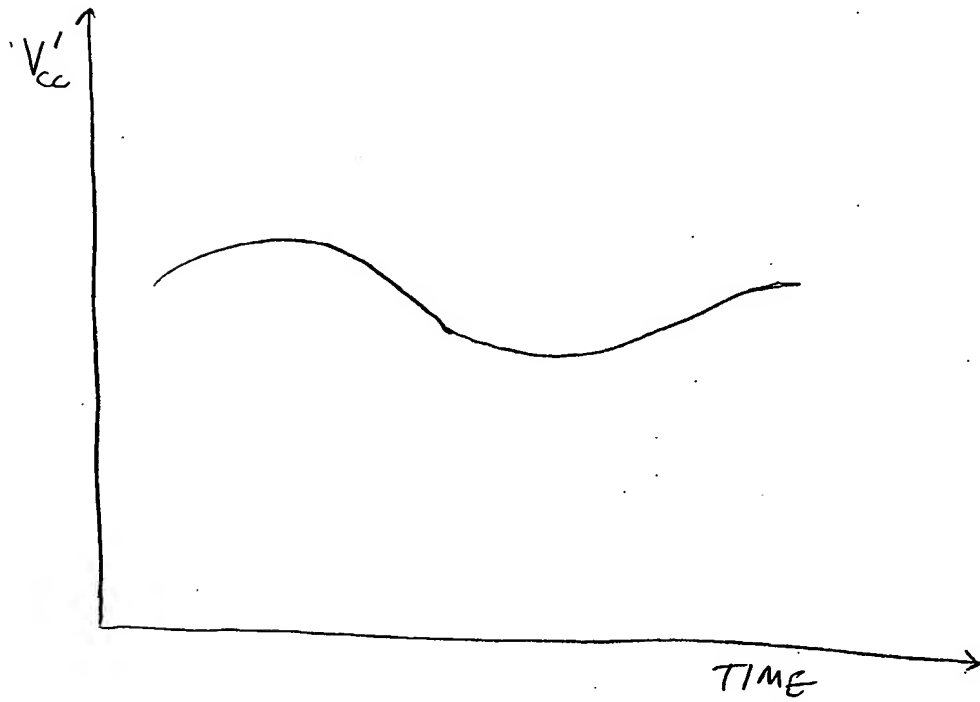


FIG. 17

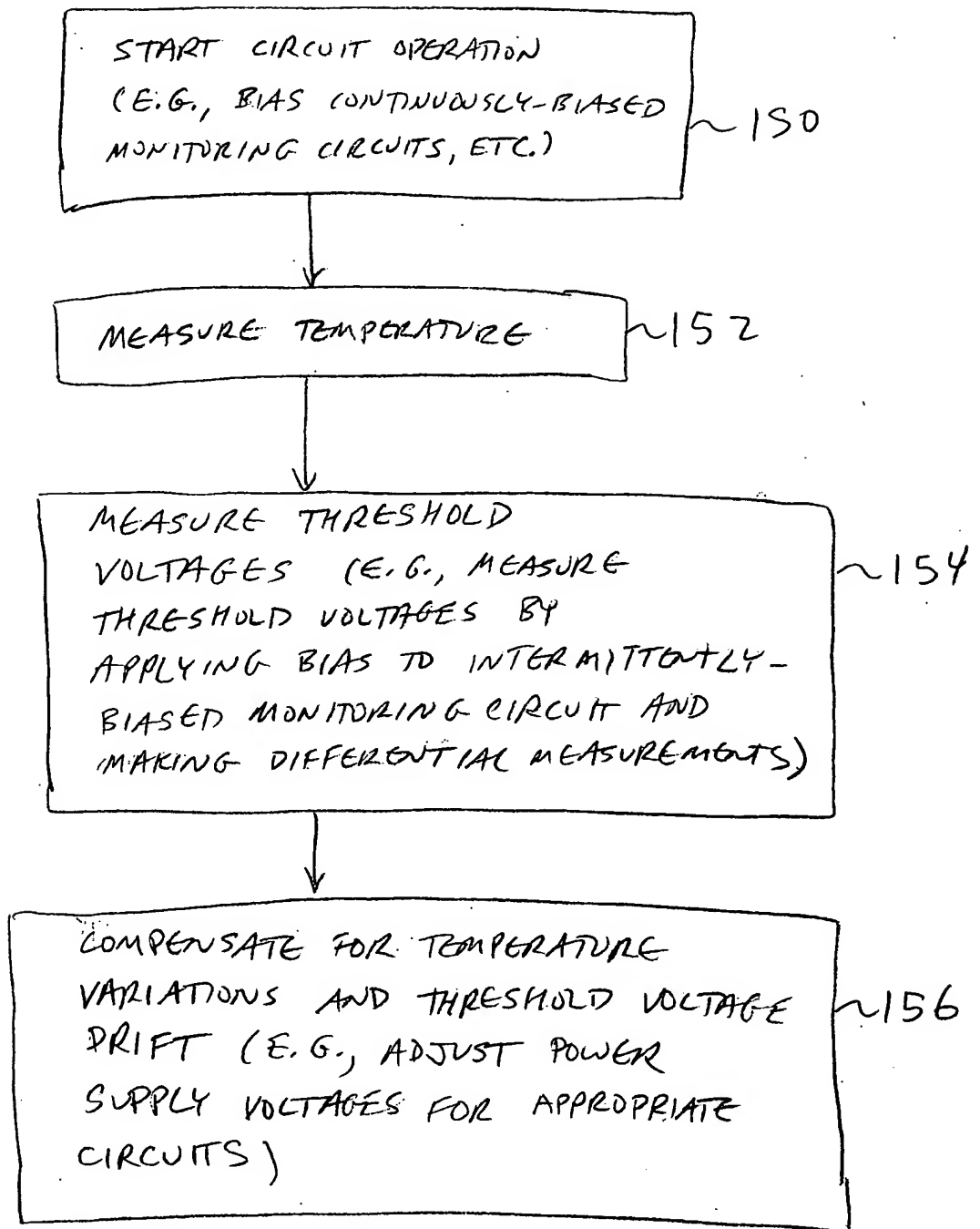


FIG. 18